ABSTRACT OF THE DISCLOSURE

The invention relates to a method for erasing non-volatile memory cells, and to a corresponding non-volatile memory device of the programmable and electrically erasable type implementing the method, and comprising a memory cell array organized in a row-and-column layout, and divided in array sectors, including at least one row decode circuit portion being supplied positive and negative voltages. The method is applied whenever the issue of the erase algorithm is negative, and comprises the following steps: forcing an incompletely erased sector into a read condition; scanning the rows of said sector to check for the possible presence of a spurious current indicating a fail state; identifying and electrically isolating the failed row; re-addressing from said failed row to a redundant row provided in the same sector; re-starting the erase algorithm.